16.1 On-Die Supply-Resonance Suppression Using Band-Limited Active Damping

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The distributed RLC characteristics of the power delivery network (PDN) constitute a complex resonance system, as show in Fig. 16.1.1. The RLC system originates in the motherboard voltage regulator and terminates on the microprocessor die. The parasitic inductance of the interconnect and the decoupling capacitors forms resonant tanks that present impedance peaks at multiple resonant frequencies. The dominant peak, which is caused by the package inductance and on-die decoupling capacitance, occurs at frequency (f_{reson}) of about 140MHz. A periodic supply current with harmonic components close to this peak can excite persistent undershoots and overshoots that exceed the droop tolerance of the supply voltage and affect operating frequency, cause hold time failures, or compromise gate oxide integrity.

Figure 16.1.2 shows an on-die resonance-suppression circuit (RSC) technique that uses band-limited active damping to reduce resonance-induced voltage fluctuations. The RSC consists of a supply noise amplifier with an integrated band-pass filter that lowers RSC sensitivity to out-of-band supply noise. The amplified supply noise in the pass band feeds a comparator that drives a current generator, which produces the damping current. When the load current has a large component close to f_{reson}, the supply voltage variation is 180° phase-shifted compared to the load current as a rising load current induces a falling supply voltage. The RSC monitors the supply voltage and generates an AC current in phase with the voltage fluctuations, or 180° out of phase with the in-band load current, effectively clamping the voltage overshoots. As a result, the load current damped with the RSC current in the resonance band is much smaller than the original load current, reducing the resonance-induced voltage noise.

Traditional techniques for resonance reduction include adding more supply pins, using C4 packages to obtain lower inductance, and adding decoupling capacitors on die to reduce the impedance of the PDN [1]. Other passive resonance suppression schemes such as introducing series resistance in the power grid [2], and adding low-Q decoupling capacitance on-die [3] to produce damping effects, have DC voltage drop problems and large area overhead. Another approach is a band-limited, active-switched capacitor scheme that dynamically configures on-die decoupling capacitors in series and shunt modes to counter resonance-induced supply noise [4]. However, capacitor-based approaches incur significant area and leakage power penalty, since MOS capacitors in advanced CMOS suffer from low area efficiency and high gate leakage. Adding special MIM capacitors to a process reduce area but increase cost. A single-shot suppressor [5] requires an additional voltage that is substantially larger than the supply voltage. In contrast, the RSC technique is simple and robust, does not use additional decoupling capacitors, and has small area overhead.

The RSC evaluation test chip, shown in Fig. 16.1.3, is fabricated in 90nm CMOS, contains the RSC, synthetic current loads and on-die decoupling capacitors. A scaled model of a microprocessor PDN is implemented by a combination of an on-die decoupling capacitor and a discrete inductor mounted on the package. The RSC band-pass filter is constructed using R_H and C_H for high-pass, cascaded through R_L and C_L for low-pass around an inverter amplifier M_1, M_2 with the virtual ground set to its switching threshold. The passive R and C elements of the filter are implemented using n-well resistors and MOS capacitors. The band-pass filter is sized for high gain in the pass-band, is centered on the power grid resonance, and has good rejection in the stop band. Filtered and amplified supply noise is fed to the inverter M_3, M_4, which acts as a comparator and a buffer driving current generator M_6. The comparator level is defined by the difference of the trip points of inverters M_1, M_2 and M_3, M_4. When the supply voltage fluctuates at a frequency close to the grid resonance, the comparator triggers the current generator. Design of the band-pass filter, choices of inverter trip points and buffer delays, and sizing of the dumping transistors together determine the effectiveness of the RSC. The RSC can be disabled to reduce the stand-by power.

Programmable step current and sinusoidal current loads are implemented on the chip (Fig. 16.1.3). The step current generator is controlled by a clock and five control bits, enabling binary-weighted current generators to set the amplitude of the step current load. The sinusoidal generator is implemented in two steps. First, the sine-cell generates approximate sinusoids using control bits from a modified Johnson counter that alternately uses positive- and negative-edge-triggered flip-flops to halve the maximum required clock frequency. Then, the binary-weighted sine-cells are arrayed and controlled by enable signals to set an amplitude of the sinusoidal current load up to 310mA.

Figure 16.1.4 shows supply noise waveforms for a sinusoidal load excitation of 3.8mA when the RSC is on and off. The peak-to-peak noise of 239mV is suppressed to 55mV after the RSC is enabled, which is a 12.76dB reduction. To evaluate effectiveness of the RSC in the interest range of the PDN impedance, we select three discrete inductors of 13, 24, and 51nH to set the resonant frequency to 188, 140, and 100MHz, respectively. In each resonance band, we repeat peak-to-peak noise measurements by sweeping excitation frequencies from 50 to 360MHz (Fig. 16.1.5). To excite noise away from each resonance peak, the amplitude is increased to 5mA. When the RSC is on, the peak-to-peak noise drops to about 100mV for frequencies within the pass-band of the RSC filter.

RSC power consumption is due to the bias current for the inverter amplifier and the damping current through the current generator (Fig. 16.1.6). The damping current is proportional to the excitation current injected in the PDN. At f_{reson}, 1mA of active damping current is drawn per 3mA of load current. The measured RSC current due to the damping action is in agreement with the calculated current assuming an ideal damping circuit.

Figure 16.1.7 shows the die micrograph. The RSC occupies 59×20μm^2. The noise-cancellation current density of the RSC is 8.5A/mm^2, which is 17× larger than the density of 0.5A/mm^2 reported in the switching capacitor approach [4]. The RSC consumes a quiescent current of 2.42mA, which is reduced to 0.85mA by increasing the inverter skew and adding another inverter gain stage. For a 100mm^2 processor chip, applying RSC to the non-cache portion requires 0.9mm^2 and consumes 1.94W of static power and up to 2.16W noise-cancellation power with a maximum of 12.76dB resonance reduction. With the quiescent-current-reducing techniques, the static power can be reduced to 0.68W.

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[2] D. Blaauw, et al., Design of High-Performance Microprocessor Circuits, edited by A. Chandrakasan, et al., IEEE Press 2001.
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[5] L. Amoroso, M Donati, M. Zyou, and F.C. Lee, "Single Shot Transient Suppressor (SSTS) for High Current High Slew Rate Microprocessor," *Applied Power Electronics Conf. and Exposition*, vol. 1, pp. 284 -288, Mar., 1999.

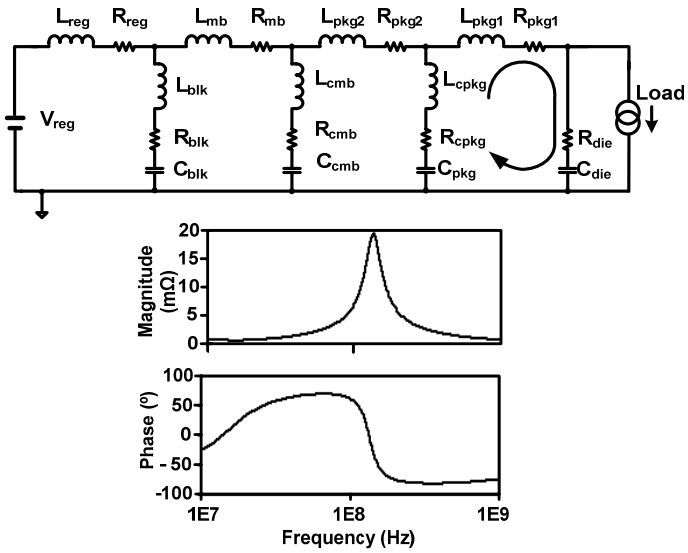

Figure 16.1.1: Diagram of PDN, impedance magnitude and phase plots.

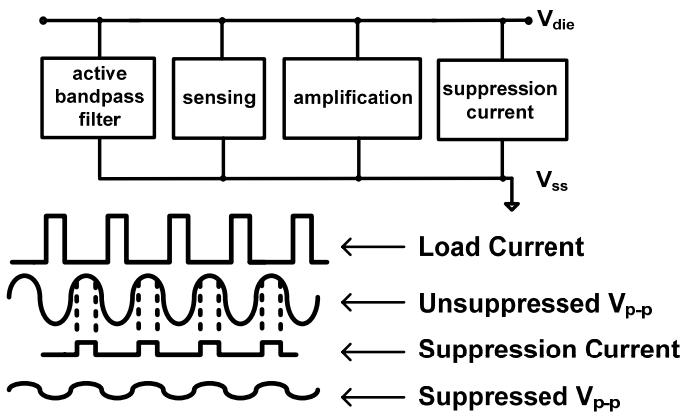

Figure 16.1.2: Basic block diagram of RSC and illustration of the RSC principle.

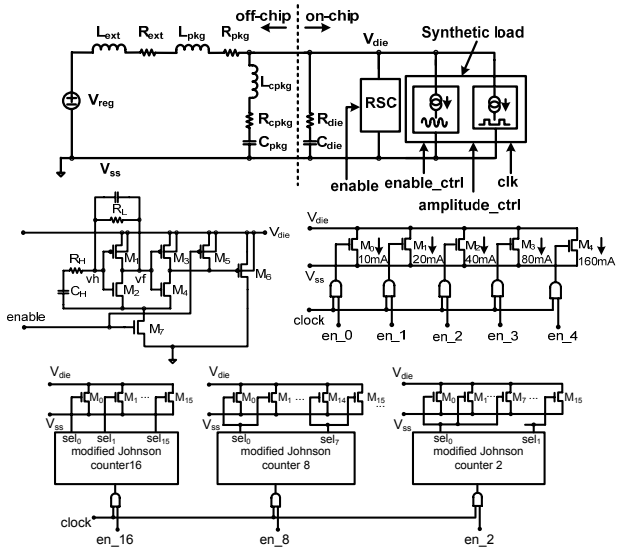

Figure 16.1.3: Testchip block diagram, RSC circuit, and synthetic load schematics.

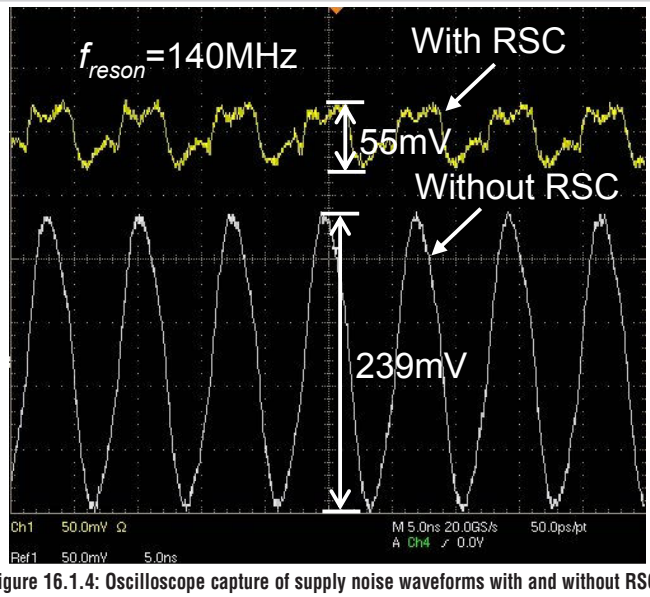

Figure 16.1.4: Oscilloscope capture of supply noise waveforms with and without RSC.

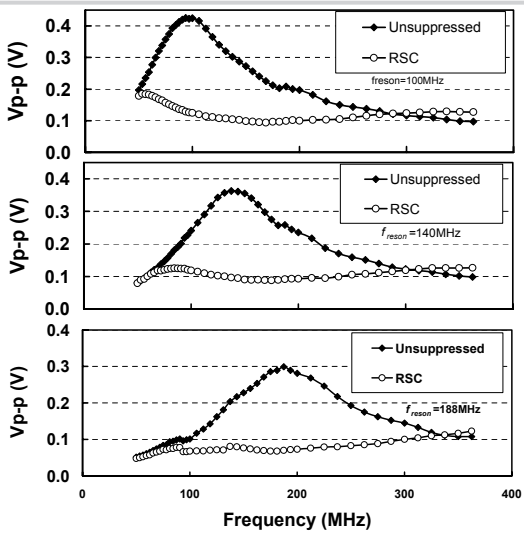

Figure 16.1.5: Measured peak-to-peak noise vs. frequency with and without RSC at different resonant frequencies.

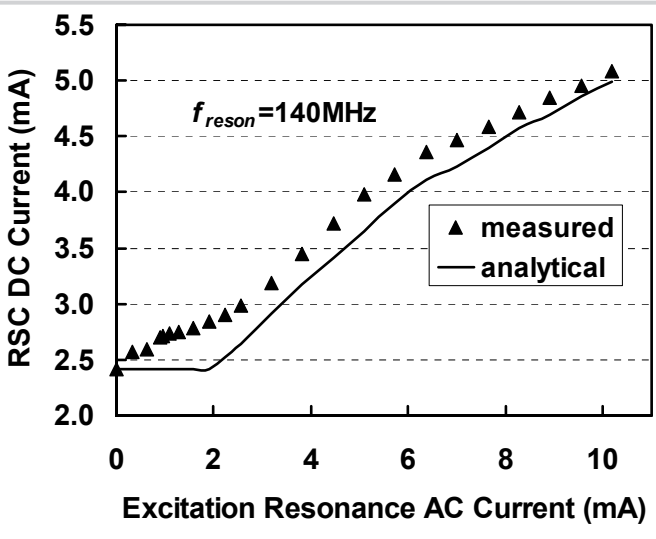

Figure 16.1.6: Measured and analytical RSC current vs. excitation resonance AC current.

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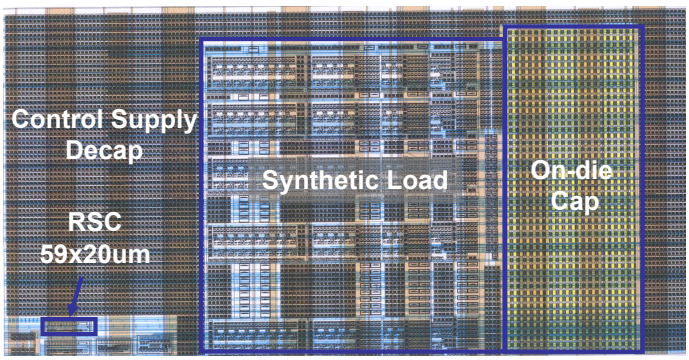

Technology	90nm CMOS	Max resonance reduction	12.76dB
Total die area	1042x447μm²	Suppression current density	8.5A/mm²
RSC Area	59x20μm²	Resonance suppression frequency	70 – 250MHz

Figure 16.1.7: Die micrograph and characteristic summary table.

